Docket No.: 071971-0566

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 53080

Tsuyoshi MATSUSHITA

Confirmation Number: Not Yet Assigned

Application No.: 10/575,098

Group Art Unit: Not Yet Assigned

Filed: April 10, 2006

Examiner: Not Yet Assigned

For: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING THE

SAME

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The Customer Number for the above listed application should be:

53080

It is requested that the U.S. Patent and Trademark Office records be updated to reflect this correction. Thank you.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty Registration No. 36,139

600 13th Street, N.W. Washington, DC 20005-3096

Phone: 202.756.8000 MEF:ln Facsimile: 202.756.8087 Date: September 13, 2007

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| Applicant: | Tsuyoshi N | MATSUS | HITA | | | | Do | cket No. | 071 | 971-05 | 66 | | | Serial No. | Not Yet | Assigned |
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Tsuyoshi MATSUSHITA Confirmation Number: Not Yet Assigned

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SAME

LETTER TO SUBMIT FRONT PAGE OF INTERNATIONAL PUBLICATION AND ENGLISH-TRANSLATED INTERNATIONAL SEARCH REPORT

Mail Stop OIPE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Attached are copies of the front page of the International Publication and the English translation of the International Search Report received from the International Bureau of WIPO for the corresponding PCT application of the above-referenced application. It is requested that the U.S. Patent and Trademark Office records be updated to include these documents. Thank you.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

Phone: 202.756.8000 MEF:In Facsimile: 202.756.8087 Date: September 13, 2007

Washington, DC 20005-3096

600 13th Street, N.W.

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(12) 特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関 国際事務局



発信:前田特許事務所

(43) 国際公開日 2006 年8 月 24 日 (24.08.2006)

PCT

(10) 国際公開番号 WO 2006/087845 A1

- (51) 国際特許分類: H03K 19/0185 (2006.01)
- (21) 国際出願番号:

PCT/JP2005/019780

(22) 国際出願日:

2005年10月27日(27.10.2005)

(25) 国際出題の言語:

日本語

(26) 国際公開の言語:

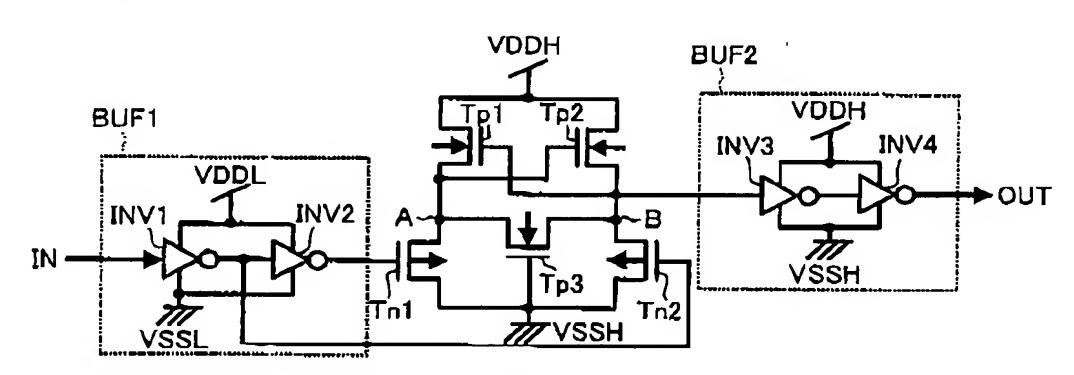
日本語

- (30) 優先権データ: 特願2005-041291 2005年2月17日(17.02.2005) JF
- (71) 出願人(米国を除く全ての指定国について): 松下電器産業株式会社 (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) [JP/JP]; 〒5718501 大阪府門真市大字門真1006番地 Osaka (JP).
- (72) 発明者; および
- (75) 発明者/出願人 (米国についてのみ): 松下 剛 (MAT-SUSEUTA, Tsuyoshi).

- (74) 代理人: 前田 弘 , 外(MAEDA, Wroshl et al.); 〒5410053 大阪府大阪市中央区本町2丁目5番7号 大阪丸紅ビル Osaka (JP).
- (81) 指定国 (表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) 指定国(表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LY, MC, NL, PL, PT, RO, SE, SI, SK, TR),

/銃葉有]

- (54) Title: LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT HAVING THE SAME
- (54) 発明の名称: レベルシフト回路及びこれを備えた半導体集積回路



(57) Abstract: A level shift circuit comprising two N-ch transistors (Tn1,Tn2) that receive a pair of complementary input signals; and two P-ch transistors (Tp1,Tp2) that have their gate terminals cross-coupled to each other; wherein nodes (A.B), which are the drains of the two N-ch transistors (Tn1,Tn2) and which operate inversely to each other, are connected to each other at a resistor (Tp3). The resistor (Tp3), which comprises a P-ch transistor, has its gate grounded and is always conductive. For example, when the N-ch transistor (Tn1) is turned on and the N-ch transistor (Tn2) is turned off, a current initially flows from the node (A) exhibiting a higher potential through the resistor (Tp3) to the node (B) exhibiting a lower potential, which results in a rise of the potential at the node (B). Therefore, the potential rise at the node (B) is promoted as compared with a case where only the P-ch transistor (Tp2) is turned on. Thus, the level shift circuit having a less number of elements can operate in a higher rate.

(57) 要約: レベルシフト回路において、一対の相補入力信号を受ける2つのNchトランジスタ Tn 1、Tn 2と、ゲート端子が互いにクロスカップル接続された2つのPchトランジスタ Tp 1、Tp 2とを備えたレベルシフト回路において、前記2つのNchトランジスタ Tn 1、Tn 2のドレインであって互いに反転動作しているノードA、日間士が、抵抗 Tp 3で接続される。この抵抗 Tp 3は、Pchトランジスタで構成され、そのゲートは接地されて、常時導通状態にある。例えば、Nchトランジスタ Tn 1がONし、Tn 2がOFF する際には、その当初で、高電位側のノードAから電流が抵抗 Tp 3を通じて低電位側のノード日に流れて、低電位側のノード日の電位上昇は、Pchトランジスタ Tp 2のONのみによる場合に比べて促進される。従って、このノード日の電位上昇は、Pchトランジスタ Tp 2のONのみによる場合に比べて促進される。従って、レベルシフト回路を少ない素子数でもって高速動作できる。



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OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類: 一 国際調査報告書

2文字コード及び他の略語については、定期発行される 各PCTガゼットの巻頭に掲載されている「コードと略語 のガイダンスノート」を参照。

発信:前田特許事務所

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International application No.

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